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(71) Applicant: International Business Machines Corporation
Old Orchard Road
Armonk, N.Y. 10504(US)

(72) Inventor: McBride, Donald Gene
2058 Cheshire Road
Binghamton, N.Y. 13 903(US)
Inventor: Shaw, Jane Margaret
49 Old Sib Road
Ridgefield, Conn. 06 877(US)

(74) Representative: Kreidler, Eva-Maria, Dr. rer. nat.
IBM Deutschland GmbH Patentwesen und Urheberrecht Schönaicher Strasse 220
D-7030 Böblingen(DE)

(54) Organic solder barrier for a semiconductor device.

(57) A method for defining a solder barrier using a silylated positive photoresist is disclosed.

The silylated positive photoresist layer replaces the top chrome layer previously employed and defines the solder barriers and I/O select patterns. The personality pattern in the Cr-Cu layers is defined by the use of a positive photoresist which is etched to provide the copper etch mask. The etched copper is then used to etch the chrome. This avoids the incompatibility of the positive photoresist with the alkaline chromium etchant.

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ORGANIC SOLDER BARRIER

This invention relates to a process for defining a solder barrier utilizing a silylated photoresist. In joining a semiconductor chip to a substrate, a solder joint is employed to provide the necessary electric coupling between the microminiature semiconductor component and terminal metallurgy on the substrate surface. This invention is directed to a process and the resulting structure of employing a high temperature organic solder dam to isolate the terminal area on the substrate from the overflow of solder during the joining operation.

In the manufacture of semiconductor devices, a number of semiconductor chips are joined to a substrate. Typically, solder contacts are employed. Such are shown in U.S. Patents 3,392,442 and 3,495,133. The solder ball, generally comprising a solder alloy of tin and lead collapses in a controlled manner to provide the necessary connection. During this controlled collapse of the solder ball, it is necessary to provide a stop-off or solder dam to prevent solder material from spreading and typically running down the circuit line.

In the 3,392,442 patent, the solder mounds are deposited respectively on a composite of contact metallization which comprises layers of chromium, copper, and gold which are vacuum deposited to provide the desired electrical contact to aluminum land 26. It is recognized in the art that the chromium deposit is necessary to establish the necessary isolation of the contact area such as clearly is illustrated in Figure 3 of the 3,392,422 patent.

Reference is made to IBM Technical Disclosure Bulletin, Volume 16, No. 11, pp. 3610-3611 (April 1974). This TDB discloses techniques of joining semiconductor chips to a substrate by means of a lead-indium solder joint. It is recognized, where controlled collapse chip connections (C4) are employed, isolation of the terminal area is required. Consequently, glass is used in one embodiment, chromium in another, ceramic in a third and silicon dioxide in a fourth implementation of the isolation structure.

In another known process, chromium-copper-chromium blankets are successively deposited onto the substrate. The deposition may be vacuum deposition or sputtering. The first layer of the chromium acts as an adhesion barrier between the copper layer and the ceramic or polyimide forming the substrate material. The intermediate copper layer is the conducting circuit layer as in the case of the 3,392,442 patent. The top chromium layer is employed as the solder stop-off or solder dam layer. Thus, as in the case of the 3,392,442 patent, this solder dam prevents run off of solder from the solder ball forming the C4 interconnection from contaminating adjacent portions of the substrate. Typically, the solder during collapse tends to run down the circuit line of the chip to be interconnected, thereby ruining that chip. Consequently, as recognized in the art, the top chromium layer is the key to having control collapse of the solder ball in achieving positive chip connection without run-off.

In accordance with this technique and by the extension of that described in the 3,392,442 patent, circuitization of the blanket layers, that is chromium-copper-chromium requires two complete photolithographic and etching processes. The first step defines the circuitry, or personalization and the second creates the solder dam. The second step is, therefore, a select etch. The photoresist of choice is currently KTFR (trademark of Kodak Co.), a negative photoresist which comprises a partially cyclized poly-cis-isoprene with an average unsaturation of one double bond per 10 carbon atoms and 2,6-bis(p-azidobenzylidene)-4-methylcyclohexane as sensitizer compound. Etchant of choice is $KMnO_4/KOH$ as a chromium etchant and $FeCl_3/HCl$ as the copper etchant.

One of the difficulties in using this choice of materials is the inability of achieving fine line resolution. Another problem is that of stripping. Consequently, within the technology, there exists a limitation on line resolution which may be achieved and, therefore, overall density of the device. The potential use of a positive photoresist would provide a solution. However, a positive photoresist cannot be used because it is incompatible with the use of the top chromium layer. The incompatibility is that when the chrome layer is etched the positive photoresist will also be etched in the same step. Thus, given the use of chromium, the only reliable etchant used to date has been $KMnO_4/KOH$.

Another problem with the use of a negative photoresist such as KTFR is the use of the particular stripping material. J100 (trademark of Indust-Ri-Chem Lab., Richardson, Texas) which comprises the Na-salt of an alkyl naphthalene sulfonate, free sulfonic acid, and tetrachloroethylene, o-and p-dichlorobenzene, and phenol, is currently employed. This material is considered aggressive and presents environmental and health problems. Moreover, it must be used under extremely controlled conditions to prevent yield losses on the product.

Consequently, given the limitations in the technology, the definition of a system which would allow the use of a positive photoresist offers numerous advantages. However, to use standard positive photoresists, the requirement of top level chromium as a solder dam must be eliminated.

This is because chromium is etched by basic solutions such as NaOH or KOH which, in use would be destructive to the positive photoresist. Consequently, there existed prior to this invention no technique by which a positive photoresist can be used compatibly with a chromium solder dam layer.

Given these deficiencies in the prior art, the object of this invention is a technique of depositing a high temperature organic solder dam and the resulting package structure. The object of the invention is achieved according to claims 4 and 1.

This invention employs a silylated photoresist. Such a photoresist comprises a plasma-resistant polymeric material which is prepared by reacting a polymeric material containing reactive hydrogen functional groups with a multifunctional organometallic material containing at least two functional groups which are reactive with the reactive hydrogen functional groups of the polymeric material. Such a material can be hexamethylcyclotrisilazane. A silylated photoresist of this type suitable for this invention is described in detail in U.S. Patent Application Serial No. 713,509, entitled "Plasma-Resistant Polymeric Material, Preparation Thereof and Use Thereof", filed on March 19, 1985 by Babich et al (= EP-A 0 198 215). This disclosure of that commonly assigned patent application is expressly incorporated herein by reference.

This invention, therefore, is directed to a specific use of a silylated photoresist as a solder dam layer joining of semiconductor devices to a substrate. This material is used in place of the chromium layer in the process described herein.

In accordance with this invention, a semiconductor substrate is provided with a blanket Cr-Cu deposition. The positive photoresist is then blanket covered over the Cr-Cu layer. The photoresist is then exposed and developed to obtain the necessary personalization. Metallization lines defining the circuitry are then defined by appropriate etching. The positive photoresist is then stripped followed by etching the bottom chromium layer. The solder dam is then created by reapplying a second positive resist pattern which is exposed and developed to provide the desired connection patterns. The positive photoresist is then silylated and baked. In accordance with this invention, the resulting silylated photoresist is left in place to define the solder barrier.

Using this invention, improved line resolution is attained. Importantly, the requirement for top chromium is eliminated. This in turn reduces the number of processing steps such as top chrome etch which is required in the definition of the solder barrier. Moreover, the process of photoresist stripping is eliminated and this requirement for the use of aggressive and environmentally unsafe material is eliminated.

This invention will be described in greater detail by referring to the attached drawings and the description of the preferred embodiments as follows.

Figures 1 through 4 are schematic sectional views illustrating various steps in the process of this invention; and

Figure 5 is a schematic section view of a portion of a completed device illustrating the silylated photoresist in place as a solder dam.

Description of the Preferred Embodiment

Referring now to Figures 1 through 4, the process in accordance with this invention is illustrated. Figure 1 illustrates a portion of a substrate that has received intermediate processing. As illustrated in Figure 1 onto a substrate 10 a blanket layer 14 of chromium and a blanket layer 16 of copper are deposited. A positive photoresist 18 is deposited over the chromium copper layers 14 and 16. Figure 1 illustrates the exposure, development and etching of the positive photoresist 18 to define the personality pattern.

With this intermediate structure then defined, the copper layer 16 is etched with an appropriate copper etchant. Such is illustrated in Figure 2. Thus, the openings 20 and 22 which define the personality pattern extend through the copper layer 16 and terminate at the chromium layer. An appropriate copper etchant is $FeCl_3/HCl$, $CuCl_2$ or the like. Following this definition of the personality pattern the photoresist is stripped away with an appropriate stripper. Then, using the etched copper as a mask, the bottom chromium layer 14, is etched in appropriate chromium etchant. Such may be $KMnO_4/KOH$ or any appropriate chromium etchant. Alternatively, the chromium may be etched with the positive photoresist layer in place, that is, immediately following copper etch, but prior to stripping of the resist layer however, the chromium etchant may remove the positive photoresist.

Figure 3 illustrates the next salient intermediate step in accordance with this invention. The second layer of a positive photoresist 24 is blanketly applied over the copper layer 16 filling the openings 20 and 22. This photoresist 24 is then exposed and developed to provide the select patterning for the solder barriers, I/O (input/output) patterns and the like. Those openings 25 are illustrated in Fig. 4 as to the select pattern where the solder dams are placed. The positive photoresist is then silylated

and baked. This is accomplished in accordance with techniques which are disclosed in the aforementioned U.S. application Serial No. 713,509 which has been incorporated herein by reference.

It is noted that the silylated photoresist is left in place as the solder barrier. Processing then occurs in accordance with established techniques such as described in U.S. Patent 3,392,442. That is, solder is deposited into openings 25 via immersion in a molten solder bath or the like. Such is well known in the technology. Alternatively, solder need not be deposited in openings but may be delivered to the interconnection site by the chip. The resulting structure is illustrated in Figure 4. Next, the chip is joined to the solder connections, that is to connection 28. This is illustrated in Fig. 5 and represents the final product.

The presence of the silylated photoresist 24 acts as a barrier affirmatively preventing the solder reflow from running down the circuit lines thus causing collapse of the chip which may result in the shorting of the chip to the substrate. As can be appreciated the requirement previously existing in the technology for top chromium is eliminated by this invention. Also, given the use of a positive photoresist fine line resolution capability is achieved.

Figure 5 illustrates the silylated photoresist remaining on the total surface of the substrate. Alternatively, silylated photoresist may be selectively removed once solder barriers are defined by the necessary dams for the solder connections. Advantages, however, occur by allowing the silylated photoresist to remain on the top surface. Corrosion protection over both the circuit lines and the bare copper edge of the circuit lines occurs. Additionally, dip tinning is possible because bridging of fine lines will not occur.

It is apparent that other improvements and advantages of this invention will be appreciated and modifications may be practiced without departing from the essential scope of this invention.

Claims

1. Electrical connection between a semiconductor chip and a carrier comprising:

a reflow solder ball contacting said chip and said carrier; and

a silylated positive photoresist layer surrounding said solder ball on the surface of said carrier to act as a solder dam.

2. Electrical connection of claim 1, wherein said silylated positive photoresist covers the entire surface of said carrier.

3. Electrical connection of claim 1, wherein said silylated positive photoresist covers only conductive circuit lines on the surface of said carrier.

4. Method of making a solder barrier for a chip carrier comprising the steps of:

blanket coating said carrier with layers of chromium and copper,

blanket coating said copper layer with a positive photoresist,

exposing and developing said photoresist to define a personality pattern followed by etching said copper layer,

etching said chromium layer using said etched copper layer as a mask,

applying a second blanket layer of positive photoresist on to said etched copper and chrome layers,

exposing and developing said second layer of positive photoresist to define a select pattern, and

silylating said second layer of positive photoresist followed by baking.

5. Method of claim 4 further comprising the step of placing solder at locations on the select pattern.

6. Method of claim 5 further comprising the step of joining a chip to said carrier.

7. Method of claim 6, wherein said chip is joined by the controlled collapse chip connection of the solder.

8. Method of claim 4 further comprising the step of removing the silylated photoresist from selected portions on the chip carrier.

9. Method of claim 4 further comprising the step of removing the first layer of positive photoresist prior etching of the chromium layer.

10. Method of claim 4, wherein said copper layer is etched with $FeCl_3/HCl$ or $CuCl_2$.

11. Method of claim 4, wherein said chromium layer is etched with $KMnO_4$.

FIG.1

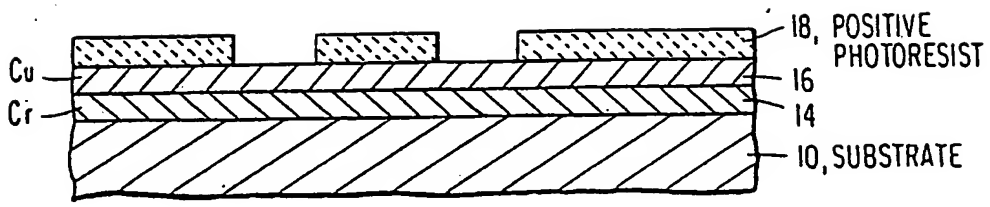

FIG.2

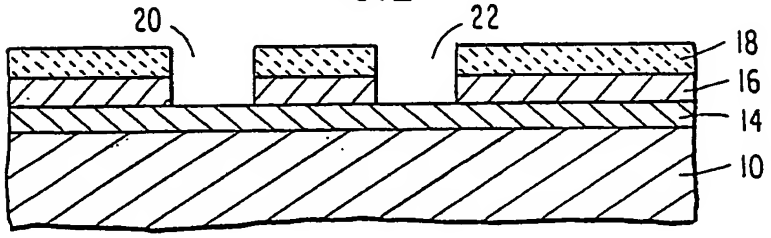

FIG.3

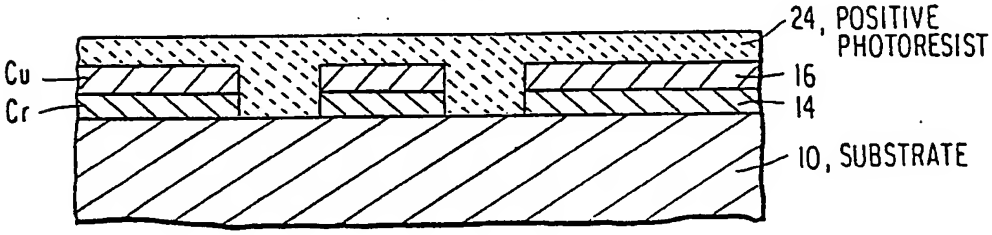

FIG.4

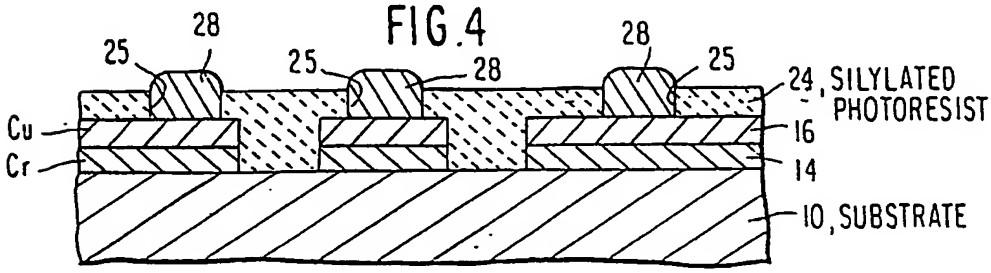

FIG.5